IN THE CLAIMS:

Please amend claims 1, 3-5, 7, 9, 11, 12, 16 and 25 as indicated in the following.

Please cancel claims 6, 14, 18 and 28 without prejudice as indicated in the following.

Please add claims 33-35 as indicated in the following.

Claims Listing:

1. (Currently Amended) A method comprising:
receiving a single digital data stream;
encrypting[[,]] a first portion of the single digital data stream with a first encryption key to generate a first encrypted stream; and
encrypting a second portion of the single digital data stream with a second encryption key to generate a second encrypted stream.

2. (Original) The method as in Claim 1, wherein encrypting the first portion of the single data stream and encrypting the second portion of the single data stream is performed by a single encryption component.

3. (Currently Amended) The method as in Claim 1, wherein the first encryption key is generated using a public encryption key associated with a peripheral device, a set of private keys associated with the peripheral ~~controller~~device, and a first pseudo random number and further wherein the second encryption key is generated using the public encryption key associated with the peripheral device, the set of private keys associated with the peripheral ~~controller~~device, and a second pseudo random number.

4. (Currently Amended) The method as in Claim 1, further including ~~the steps of~~:
receiving the first and second encrypted streams;
decrypting the first encrypted stream to generate a first portion of a received data stream;
decrypting the second encrypted stream to generate a second portion of the received data stream;

combining the first portion of the received data stream with the second portion of the received data stream to generate a single received data stream.

5. (Currently Amended) The method as in Claim 4, further including ~~the step of~~:
receiving a display enable signal, a horizontal sync signal, a vertical sync signal, and a clock signal.

6. (Canceled)

7. (Currently Amended) The method as in Claim 5, wherein the second [[seed]]encryption key is regenerated according to the horizontal sync signal.

8. (Original) The method as in Claim 5, wherein the encryption is re-keyed according to a trigger from the horizontal sync signal.

9. (Currently Amended) The method as in Claim 1, wherein the single data stream is associated [[to]]with video display data.

10. (Original) The method as in Claim 9, wherein the first portion of the single data stream is associated with even pixels and the second portion of the single data stream is associated with odd pixels.

11. (Currently Amended) The method as in Claim 1, wherein the single data stream ~~runs at twice the speed~~has a data rate that is twice a data rate of the first and second encrypted streams.

12. (Currently Amended) A system comprising:

a data processor having a first I/O buffer;

a memory having a second I/O buffer coupled to the first I/O buffer of the data processor, the memory capable of storing code for:

establishing a set of encrypted links between a peripheral device and a software component, wherein establishing [[the]]a first encrypted link of the set of encrypted links includes generating a first encryption key associated with a first port of encrypted data and establishing [[the]]a second encrypted link of the set of encrypted links includes generating a second encryption key associated with a second port of encrypted data;

a hardware controller capable of outputting the first and the second encrypted links, wherein the hardware controller includes:

a first register capable of storing information associated with the first encryption key;

a second register capable of storing information associated with the second encryption key;

a cipher component[[,]] capable of :

~~interweaving~~ receiving a single digital data stream;

applying the first encryption key to a first portion of the data stream; and

applying the second encryption key to a second portion of the data stream; and

a de-multiplexing component capable of splitting the single data stream into multiple data streams.

13. (Original) The system as in Claim 12, further including:

a multiplexing component capable of:

combining the information stored in the first register with the information stored in the second register; and

providing the combined information to the cipher component;

a clock capable of clocking data bits from the single data stream; and

a half speed clock capable of clocking data in the multiple data streams.

14. (Canceled)

15. (Original) The system as in Claim 12, wherein the cipher component applies the first encryption key to even bits in the single data stream and applies the second encryption key to odd bits in the single data stream.

16. (Currently Amended) The system as in Claim 12, further including a peripheral device comprising:

an interface capable of receiving the multiple data streams;

a first decryption component capable of decrypting a first data stream of the multiple data streams to generate a first decrypted data stream;

a second decryption component capable of decrypting a second data stream of the multiple data streams to generate a second decrypted data stream; and

a multiplexing component capable of combining the first and the second decrypted data streams to generate a single decrypted data stream.

17. (Original) The system as in Claim 16, wherein the interface is further capable of receiving a display enable signal, a horizontal sync signal, a vertical sync signal, and a clock signal.

18. (Canceled)

19. (Original) The system as in Claim 17, wherein the first and second encryption keys are regenerated according to the horizontal sync signal.

20. (Original) The system as in Claim 12, wherein the hardware controller is a video controller.

21. (Original) The system as in Claim 20, wherein the multiple data streams are received from a dual link digital video output (DVO) port on the video controller, wherein the dual link DVO port is a video interface capable of outputting two channels of data related to video.

22. (Original) The system as in Claim 21, wherein the multiple data streams are transmitted using a transmission-minimized differential signaling (TMDS) transmitter.

23. (Original) The system as in Claim 22, further including a TMDS receiver capable of receiving the transmitted data associated with the multiple data streams and outputting the multiple data streams.

24. (Original) The system, as in Claim 20, wherein the multiple data streams are received from a dual link internal TMDS transmitter and transmitted using dual-link TMDS, a video interface capable of outputting two channels of pixel data related to video.

25. (Currently Amended) A system comprising:

an interface capable of receiving a first and a second link of encrypted data from a hardware controller;

a first decryption component capable of decrypting the first link of encrypted data, using a first encryption key, to generate a first portion of a single received digital data stream;

a second decryption component capable of decrypting the second link of encrypted data[[,]] using a second encryption key[[,]] to generate a second portion of the received digital data stream; and

a multiplexing component capable of combining the first and the second portions of the received data streams to form a single received digital data stream;

26. (Original) The system as in Claim 25, further including:

a clock capable of clocking the single received data stream at twice the speed of the first and second links of encrypted data; and

a single processing component capable of processing the data associated with the first and the second links of encrypted data.

27. (Original) The system as in Claim 25, wherein the interface is further capable of receiving a display enable signal, a horizontal sync signal, a vertical sync signal, and a clock signal.

28. (Canceled)

29. (Original) The system as in Claim 27, wherein the first and the second encryption keys are regenerated according to the horizontal sync signal.

30. (Original) The system as in Claim 25, wherein the multiplexing component assigns bits of data in the first portion of the received data stream to even pixels in the received data stream and assigns bits of data in the second portion of the received data stream to odd pixels in the received data stream.

31. (Original) The system as in Claim 25, wherein the hardware controller is a video controller.

32. (Original) The system as in Claim 31, wherein the first and the second link of encrypted data are transmitted from a dual link digital video output (DVO) port on the video controller, wherein the dual link DVO port is a video interface capable of outputting two links of data related to video.

33. (New) The method as in Claim 1, wherein:

encrypting the first portion of the digital data stream includes encrypting even bits of the digital data stream with the first encryption key; and

encrypting the second portion of the digital data stream includes encrypting odd bits of the digital data stream with the second encryption key.

34. (New) The system as in Claim 12, wherein the first portion of the digital data stream is associated with even pixels and the second portion of the data stream is associated with odd pixels.

35. (New) The system as in Claim 25, wherein the first portion of the received digital data stream is associated with even pixels and the second portion of the received digital data stream is associated with odd pixels.